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AC COUPLED INTERCONNECT FOR LOW POWER SPACEBORNE ELECTRONICS

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Final Report

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14. ABSTRACT

The primary objective of this effort was to establish that AC Coupled Interconnect could be used to create multiple solutions to contactless chip-to-chip communications. Towards this goal, we took an experimental approach, developing and conducting a set of experiments showing this can be successfully achieved. In this final report, we summarize the outcomes of those experiments and list the papers, graduated students and technology transfer outcomes of this activity.

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AC Coupled Interconnect for Low Power SpaceBorne Electronics

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Introduction

The primary objective of this effort was to establish that AC Coupled Interconnect could be used to create multiple solutions to contactless chip-to-chip communications. Towards this goal, we took an experimental approach, developing and conducting a set of experiments showing this can be successfully achieved. In this final report, we summarize the outcomes of those experiments, and list the papers, graduated students and technology transfer outcomes of this activity. Technical details of everything summarized here can be found in our previous quarterly and annual reports, and the papers listed below.

Summary of Major Achievements

In this effort, we achieved the following major technology elements in ACCI:

Capacitive Coupling: Test Results of 0.18um bulk CMOS chip – wire bonded experiments . Assembly and testing of a 0.18 um bulk CMOS chip containing multiple circuit experiments. Appendix A provides details of what is on this chip. Below in Figure 1 are the chip floorplan, chip layout for the wire bonded experiments and a microscope photograph of the die. The experiments tested in this phase of measurements were in the located around the periphery of the die in the band designated in the die photo of Figure 1. A 6-bit wide ACCI Bus was demonstrated, which operates at 36Gbps or 6Gbps/channel, over 30cm transmission lines on FR4, with transceiver power dissipation less than 2mW/Gbps, while subject to crosstalk and switching noise from the simultaneous operation of 6 channels. Additional signal integrity analysis was performed to ensure it was robust to crosstalk noise and simultaneous switching noise. A summary of results achieved by this test bed are given in Table 1. A high level view of the circuit structure that was built in this demonstration is shown in Figure 2.

Circuit and System Design for Inductively Coupled Interconnect. We designed two different inductively coupled systems, one for single coupled systems, and another for dual coupled systems. The circuit diagrams for these two alternatives are illustrated in Figure 3. Several versions of the circuits for this structure are currently in IC, MCM and laminate fabrication.

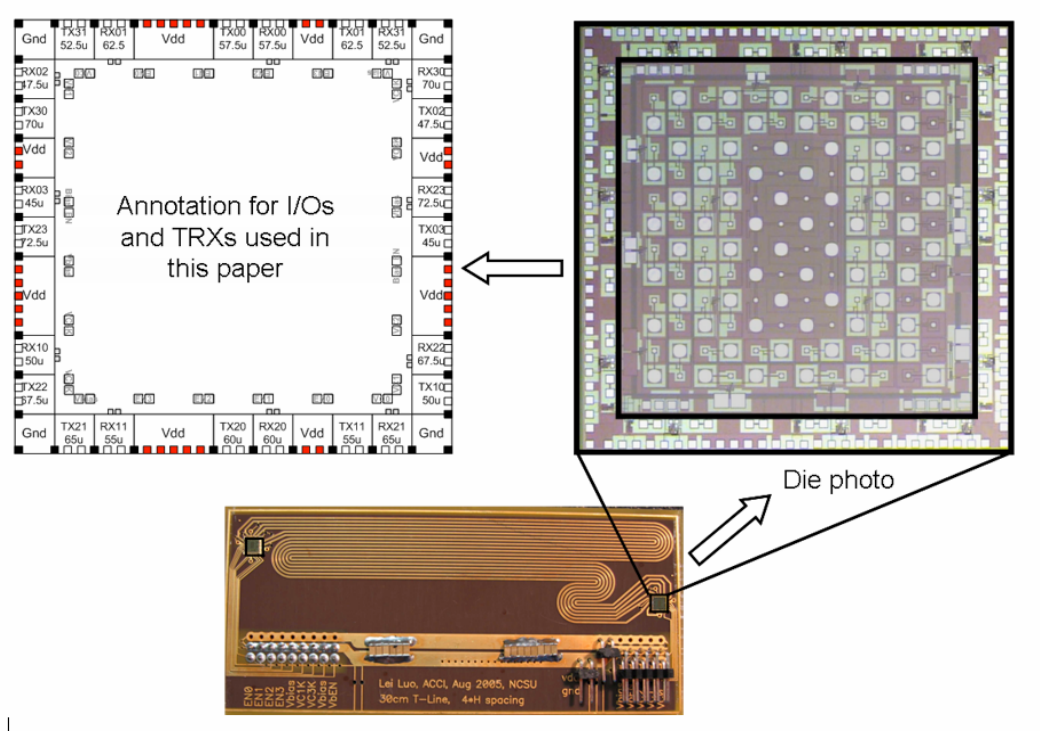


Figure 1: Chip floorplan showing wire bonded experiments, die & assembled PCB

Table I: Performance matrix

Technology		TSMC 0.18um CMOS
Area		3.5mm by 3.5mm
Power Dissipation	TX	5mw
	RX	6.8mw
	12 TRX for 72Gbps	141.6mw
	TRX Per Gbps	1.97mw/Gbps
AC signal I/Os (with TRX)	Wirebond test	12
	MCNC Flip chip test	7
	Endicott Flip chip test	7
	Total	26
Max Bandwidth	Wirebond test	72Gbps (partially measured: 36Gbps)
	Flip-chip	84Gbps
	Total	156Gbps
Max data Rate per channel		6Gbps
Min data Rate		DC (50MHZ measured, limited by source)

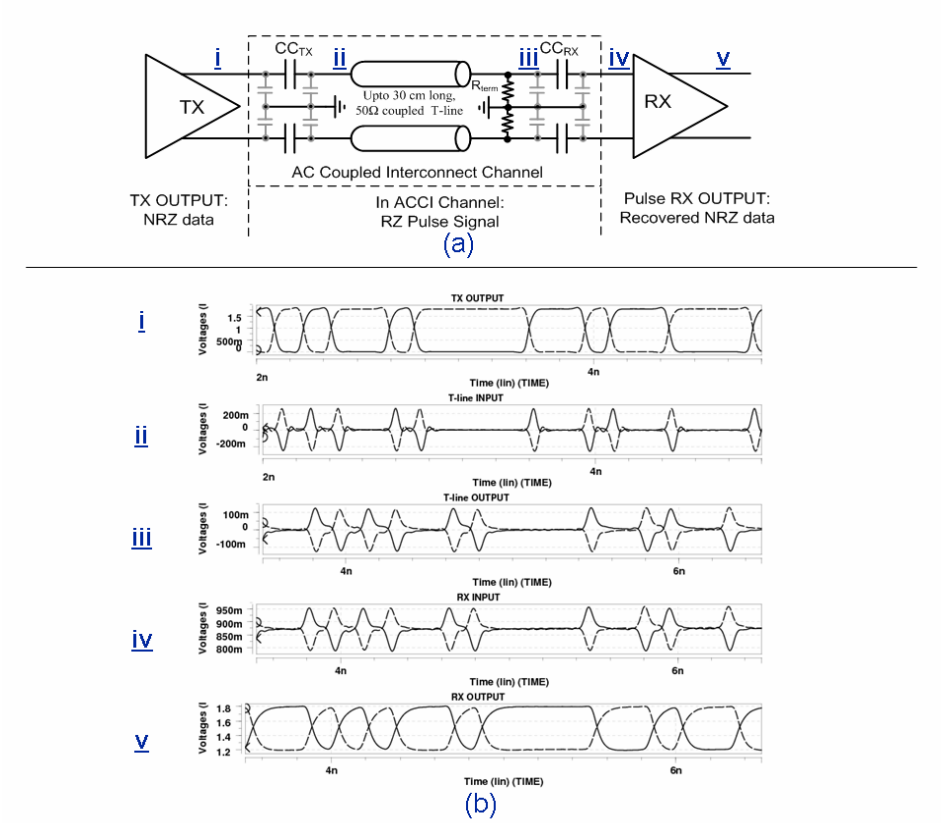


Figure 2 (a) ACCI circuit view and (b) Simulated waveforms

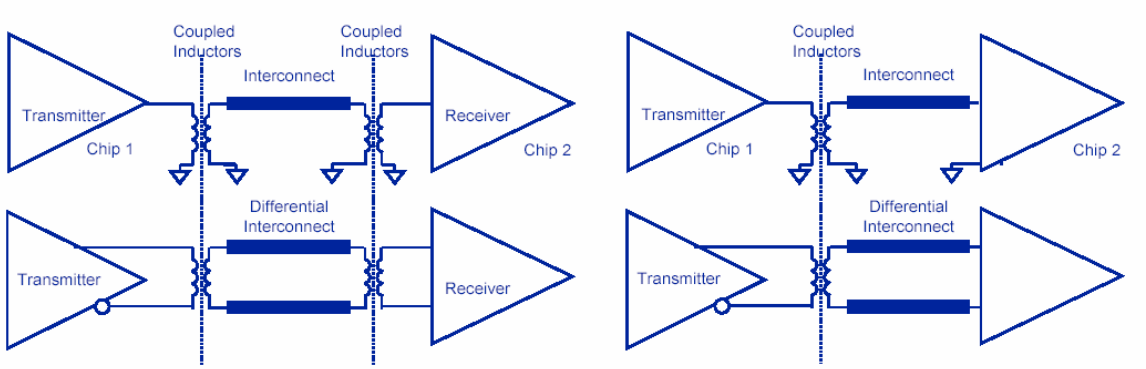
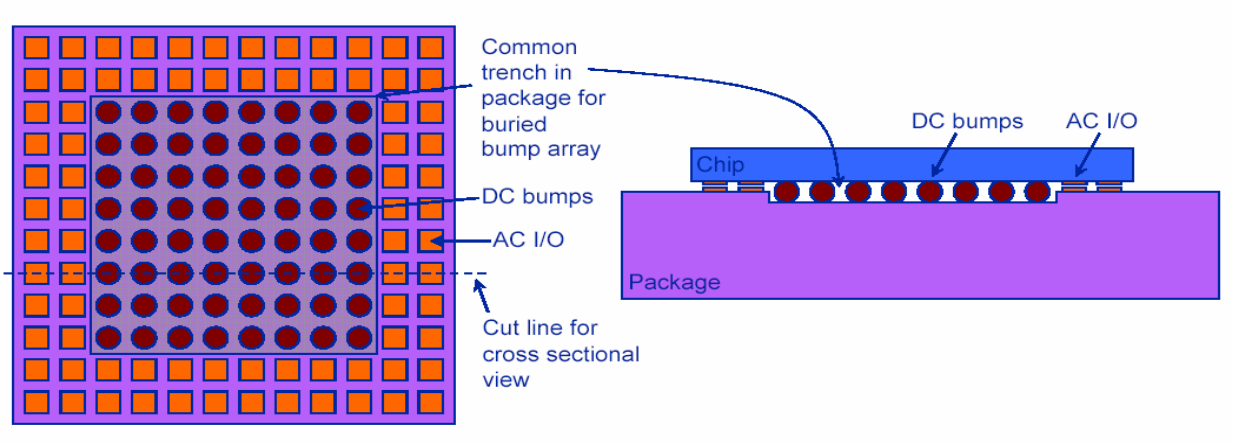


Figure 3. Left: Dual-inductively coupled structures. Right: Single inductively coupled circuit structures. The coupled inductors would be built on mated surfaces of sockets or connectors. The dual inductive structure requires a more complex circuit design than the single coupled structure, due to its complex frequency response.

Integrated Process Development for Laminate Capacitively Coupled Structures.

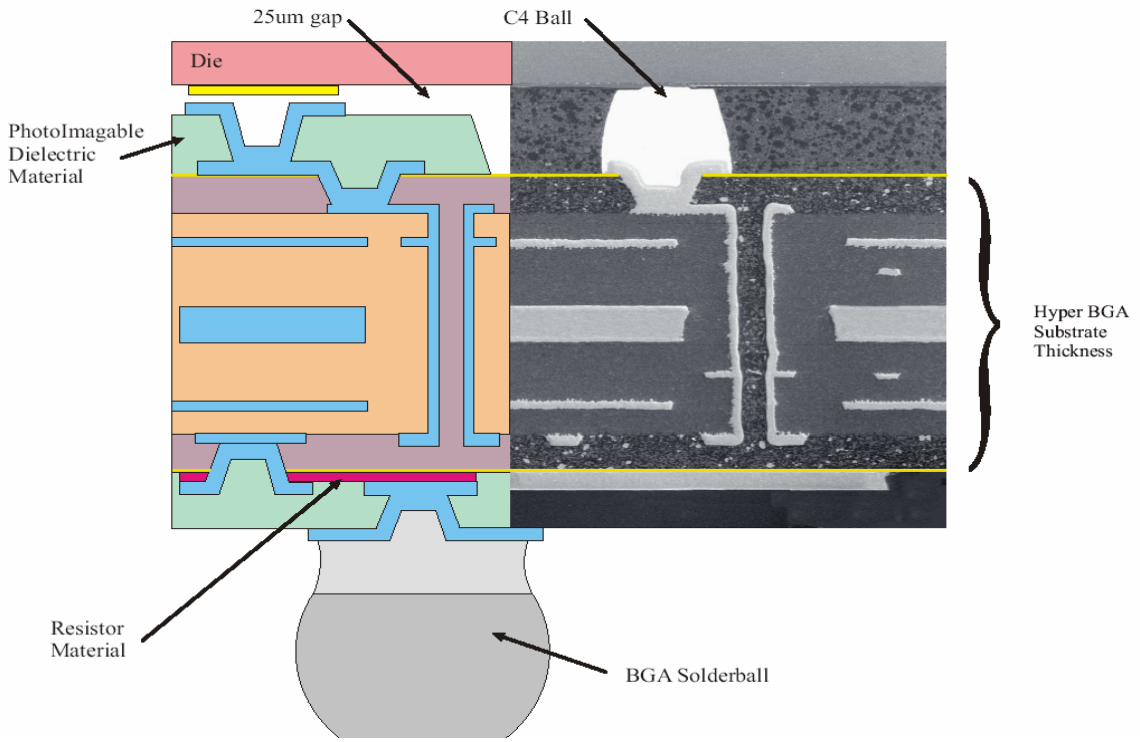
NCSU, together with EIT and RTI developed an integrated process structure that can be used to build capacitively coupled laminate packages. The key enabling technology for this structure is a patternable high-K material that can be cured at the same process temperature as solder bumps. Different versions of the material can be cured to match

the reflow profile for both leaded and lead-free solder. EIT has identified a modification to their HyperBGA product that can be used for this experiment. A high level view of the modified package structure is given in Figure 4 and a detailed view in Figure 5.



(a) (b)

Figure 4: Common trench for buried bumps in an ACCI enabled lamainate package (a) top view, (b) cross sectional view



(a) (b)

Figure 5: Endicott Laminate Package with ACCI: (a) proposed solution, (b) current solution

Design of FPGA Interface/Controller for Space-borne experiment. We completed the design, and place and route of an FPGA controller for testing an ACCI circuit on an AFRL space mission.

Integrated Package-Chip Demonstration. Demonstration of capacitive coupling with the capacitor formed between the chip and a package. We built chips in a 0.35 μm process and flipped them to an MCM substrate. We demonstrated that the chips can communicate with each other at a 2.5 Gbps over a 5 cm transmission line. Pad sizes down to 70 μm pitch were demonstrated. Figure 6 shows this package, a cross-section of it and a sample eye diagram.

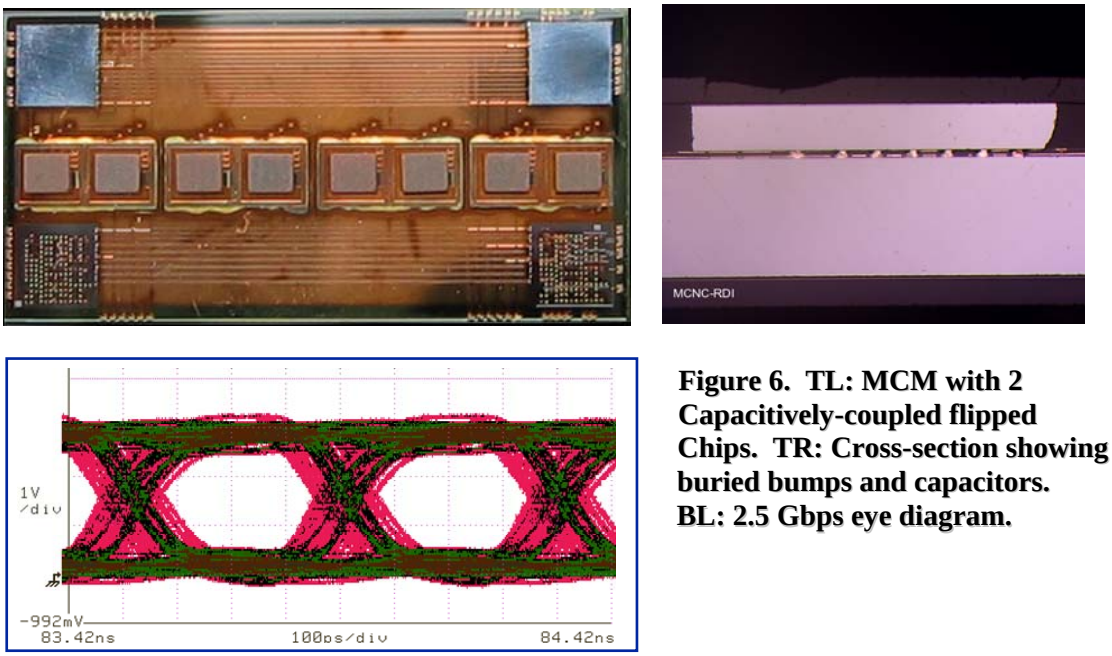
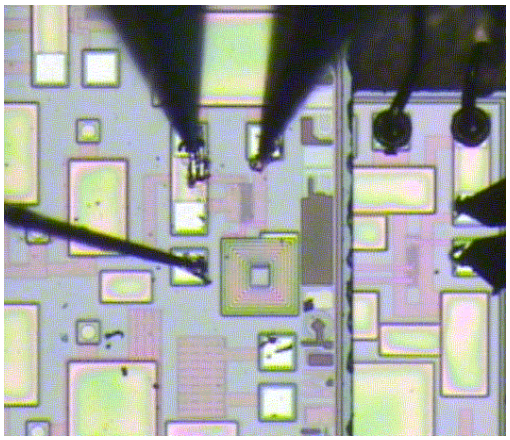


Figure 6. TL: MCM with 2 Capacitively-coupled flipped Chips. TR: Cross-section showing buried bumps and capacitors. BL: 2.5 Gbps eye diagram.

Contactless 3D Chip Stack Demonstration. Demonstration of inductively coupled circuits communicating vertically through a 3-D chip-stack. This chip was built in a 0.35 μm process and operated at 2 GHz. Communication was possible with a chip thickness of up to 120 mm. Figure 7 shows a two-chip stack and a sample eye diagram.



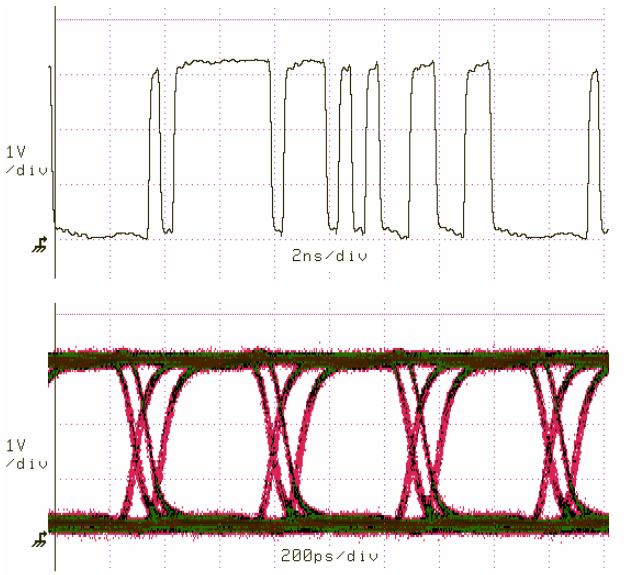
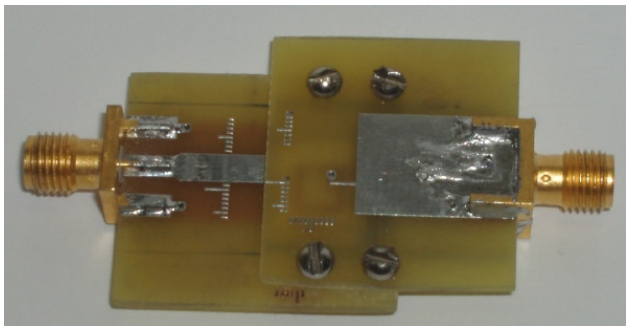


Figure 7. Two chips stacked and aligned,

Inductively Coupled Conenctor Prototype. Demonstration of an inductively coupled connector, prototyped in a cheap PCB technology and operating at 250 MHz. Figure 8 shows a prototype and an eye diagram.



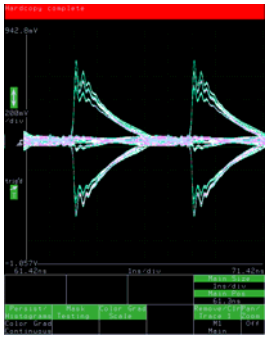


Figure 8. Scaled prototype of an inductively coupled connector, and 250 Mhz eye diagram.

Publications

The following publications have arisen because of this work:

1. L. Luo, J.Wm. Wilson, S.E. Mick, J. Xu, L. Zhang, P.D Franzon, "3 Gb/s AC coupled chip-to-chip communication using a low swing pulse receiver," IEEE JSSC, Vol. 41, No. 1, Jan 2006, pp. 287-296.
2. W.R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A.M. Sule, M. Steer, P.D. Franzon , "Demystifying 3D ICs: the pros and cons of going vertical," IEEE Design and Test of Computers, Vol. 22, No. 6, Nov-Dec. 2005, pp. 498-510.
3. J. Xu, L. Luo, S. Mick, J. Wilson, P. Franzon, "AC Coupled Interconnect for Dense 3-D ICs, "AC Coupled Interconnect for Dense 3-D ICs," in IEEE Transactions on Nuclear Science (TNS). Vol. 51(5), Oct, 2004, pp. 2156-2160.

4. S. Mick, L. Luo, J. Wilson, P. Franzon, “Buried Bump and AC Coupled Interconnection Technology, IEEE Trans. Adv.Packaging, 27(1), Feb, 2004, pp. 121-125.
5. L. Luo, J. Wilson, J. Xu, S. Mick, P. Franzon, “Signal integrity and robustness of ACCI packaged systems,“ in Proc. IEEE EPEP, Oct. 2005, pp. 11-14.
6. J. Xu, J. Wilson, S. Mick, L. Luo,“2.8 Gbps inductively coupled interconnect for 3D ICs,” 2005 symposium on VLSI circuits, June 2005, pp. 352-355.
7. K. Chandrasekar, Z. Feng, J. Wilson, S. Mick, P. Franzon,“Inductively Coupled Board to Board Connectors,“ ECTC’05, 31 May – 3 June, 2005, pp. 1109-1113.
8. J. Xu, J. Wilson, S. Mick, L. Luo and P. Franzon, “2.8 Gb/s Inductively Coupled Interconnect for 3-D ICs,” in Japan VLSI Symposium, June, 2005.
9. L. Luo, J. M. Wilson, S.E. Mick, J. Xu, L. Zhang, and P.D. Franzon, “A 3 Gb/s AC Coupled Chip-to-Chip Communication,” 2005 International Solid State Circuits Conference, San Francisco, Feb. 2005.
10. Paul Franzon, Angus Kingon, Stephen Mick, John Wilson, Lei Luo, Karthik Chandrasakhar, Jian Xu, Salvatore Bonafede, Alan Huffman, Chad Statler, Richard LaBennett, Invited Paper, “High Frequency, High Density Interconnect Using AC Coupling,” Fall MRS Conference, Boston MA, December 2003.
11. Paul Franzon, Stephen Mick, John Wilson, Lei Luo, Karthik Chandrasakhar, Invited Paper, “AC Coupled Interconnect for High-Density High-Bandwidth Packaging” Proc. SPIE, Microlectronics: Design, Technology and Packaging, Perth, Australia, December 2003. pp 67-69.
12. Paul Franzon, Stephen Mick, John Wilson, Lei Luo, Karthik Chandrasakhar, Invited Paper, “AC Coupled Interconnect for High-Density High-Bandwidth Packaging,” Japan SSDM, Tokyo, Japan, September, 2003.
13. Jian Xu, Stephen Mick, John Wilson, Lei Luo, Karthik Chandrasakhar, Paul Franzon, “AC Coupled Interconnect for Dense 3-D Systems”, Proc. IEEE Conference on Nuclear Science and Imaging, Seattle Washington, October 2003.
14. S. Mick, L. Luo, J. Wilson, P. Franzon, “Buried solder bump connections for high-density capacitive coupling,” IEEE Electrical Performance of Electronic Packaging, 2002, pp. 205-208.
15. S.E. Mick, L. Luo, J.M. Wilson, P.D. Franzon, “Buried Solder Bump Connections for High-Density Capacitive Coupling,” IEEE Electrical Performance on Electornic Packaging, October, 2002.
16. S. E. Mick, J. M. Wilson, and P. Franzon, “4 Gbps AC Coupled Interconnection,” (invited paper), IEEE Custom Integrated Circuits Conference, May 12-16, 2002, pp. 133-140.

Ph.D. and MS Students Supported

- John Wilson Ph.D., now with Rambus
- Stephen Mick, Ph.D., now with Protochips
- Lei Luo Ph.D., now with Rambus
- Karthik Chandrashekar Ph.D., now with nVidea
- Evan Erickson, still at NCSU

- Jian Xu, still at NCSU. Graduating (Ph.D.) this semester. To join ARM.
- Bruce Su, still at NCSU
- Srivatsan Parthasarathy MS**,** still at NCSU. Graduating this semester. To join Analog Devices.
- Manav Shah MS, now at Qualcomm.
- Leon Zhang Ph.D., now at IDT.
- Shep Pitts, still at NCSU
- Stephen Lipa Ph.D., graduated Dec 2005, still at NCSU as a PostDoc

Technology Transfer

Two patents have been granted (note these were both filed before receiving USAF funding):

- P. Franzon, S. Mick, J. Wilson, "Buried Solder Bumps for AC-coupled microelectronic interconnects," 6,927,490 August 9, 2005.
- P. Franzon, S. Mick, J. Wilson, "Inductively Coupled Electrical Connectors," Patent Awarded USPTO, 6,885,090, April 26, 2005.

In addition, we have developed considerable design know-how. We are currently in the following discussions regarding transferring this technology. Please keep the details conveyed below confidential.

- Rambus is interested because ACCI reduces the power consumed in high speed memory buses. We are currently in discussions with them on how to beset adapt this technology to their application.
- Endicott Interconenct Technologies is interested in ACCI because it enables large, high pin-count chips. We are working up a demonstration with them to show this potential.
- IBM is interested because of their activities in Fiber Channel. This discussion is on hold pending some internal decisions from IBM.
- Sanmina-SCT is interested because it might enable sales of some of their embedded capacitor products. We are currently in discussion with them.

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